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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

HAN, CLEMENCE S

ART UNIT PAPER NUMBER

2665

2

DATE MAILED: 11/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

S-14

Office Action Summary	Application No.		Applicant(s)	
	10/008,724		HANN ET AL	
	Examiner		Art Unit	
	Clemence Han		2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-32 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ 6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 9, 11, 13, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Munter (US Patent 5,475,679).

In regarding to claim 9, Munter teaches the multiplexer 54 receiving data from a first and second channel. Munter also teaches first and second memory banks 58 coupled to the multiplexer. Munter also teaches the scheduler 66, 70 coupled to the memory banks and operable to read out cells out of the memory banks.

In regarding to claim 11, Munter teaches a controller 60 determining the location of data storage in the memory 58 (Column 5 Line 37-38).

In regarding to claim 13, Munter teaches a Utopia bus 64 coupled to scheduler 66, 70 and the ATM switch 16.

In regarding to claim 14, Munter teaches a demultiplexer 76 coupled to the ATM switch.

In regarding to claim 15, Munter teaches the dual-port memory 58 coupled to the multiplexer and the scheduler (Column 5 Line 28).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1-5, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munter in view of Linsley (US Patent 5,583,894) and further in view of Riemann et al. (US Patent 5,892,764).

In regarding to claim 1, Munter teaches the communicating data from a first channel 50 to a first serial-to-parallel converter 52 and communicating data from a second channel 50 to a second serial-to-parallel converter 52. Munter also teaches the converting the first and second sets of data to a parallel format (Column 5 Line 13-14). Munter also teaches the writing data to memory banks 58. Munter also teaches the scheduler 66, 70 reading cells out of the memory banks 58 to an output communication link 64. Munter, however, does not teach the steps of monitoring the serial-to-parallel converters to determine when one or more words of data sets have accumulated. Linsley teaches the steps of waiting for word accumulation in serial-to-parallel converter 21 before writing data into the memory 25 (Column 7 Line 24-26). It would have been obvious to one skilled in the art to modify Munter to have the steps of waiting for the word accumulation before writing data into the memory as taught by Linsley in order to use the memory more efficiently. Munter also does not teach the steps of monitoring the memory to determine when enough

of the words have formed cells. Riemann teaches the steps of waiting for cell accumulation in the memory (Column 8 Line 64 – Column 9 Line 2). It would have been obvious to one skilled in the art to modify Munter to have the steps of waiting for the cell accumulation before reading the data out to network as taught by Riemann in order to use the network more efficiently.

In regarding to claim 2, Linsley teaches the steps of generating a memory address (Column 4 Line 55-57).

In regarding to claim 3, Munter teaches the steps of receiving cells at an ATM switch 16.

In regarding to claim 4, Munter teaches a scheduler 66, 70 coupled to the memory 58 and a Utopia bus 64.

In regarding to claim 5, Munter teaches a controller 60 determining the location of data storage in the memory 58 (Column 5 Line 37-38).

In regarding to claim 7, Munter teaches the steps of storing data in the serial-to-parallel converters 52 into memory 58 via multiplexer 54 under control of select controller 60 (Column 5 Line 14-19).

In regarding to claim 8, Linsley teaches the steps of incrementing the memory address (Column 4 Line 57-58).

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Munter in view of Linsley and Riemann et al. as applied to claim 5 above and further in view of Shimada (US 2003/0165147). Munter in view of Linsley and Riemann disclosed the steps of converting serial data to parallel data, storing the accumulated words in the memory and reading out the accumulated cells from the memory. Munter in view of Linsley and Riemann, however, does not teach the steps of sending a write enable signal to the memory. Shimada teaches the steps of sending a write enable signal to the memory [0056]. It would have been obvious to one skilled in the art to include the steps of sending a write enable signal as taught by Shimada to Munter in view of Linsley and Riemann in order to initiate the data transfer to the memory.

4. Claim 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munter in view of Hoogenboom (US Patent 6,094,430).

In regarding to claim 10, Munter teaches the multiplexer 54 receiving data from a first and second channel. Munter also teaches first and second memory banks 58 coupled to the multiplexer. Munter also teaches the scheduler 66, 70 coupled to the memory banks and operable to read out cells out of the memory banks. Munter, however, does not teach the write controllers operable to

communicate words to the multiplexer. Hoogenboom teaches the write controller 360 operable to communicate words to the multiplexer 371-374 (Column 3 Line 35-36). It would have been obvious to one skilled in the art to include the write controller as taught by Hoogenboom to Munter in order to increase the control over memory management.

In regarding to claim 12, Hoogenboom teaches the write controller 360 coupled to multiple serial-to-parallel converters 333-336 to receive data in parallel form (Column 3 Line 29-30).

5. Claim 16-20, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munter in view of Linsley and further in view of Riemann et al..

In regarding to claim 16, Munter teaches the communicating data from a first channel 50 to a first serial-to-parallel converter 52 and communicating data from a second channel 50 to a second serial-to-parallel converter 52. Munter also teaches the converting the first and second sets of data to a parallel format (Column 5 Line 13-14). Munter also teaches the writing data to memory banks 58. Munter also teaches the scheduler 66, 70 reading cells out of the memory banks 58 to an output communication link 64. Munter, however, does not teach the steps of monitoring the serial-to-parallel converters to determine when one or more words

of data sets have accumulated. Linsley teaches the steps of waiting for word accumulation in serial-to-parallel converter 21 before writing data into the memory 25 (Column 7 Line 24-26). It would have been obvious to one skilled in the art to modify Munter to have the steps of waiting for the word accumulation before writing data into the memory as taught by Linsley in order to use the memory more efficiently. Munter also does not teach the steps of monitoring the memory to determine when enough of the words have formed cells. Riemann teaches the steps of waiting for cell accumulation in the memory (Column 8 Line 64 – Column 9 Line 2). It would have been obvious to one skilled in the art to modify Munter to have the steps of waiting for the cell accumulation before reading the data out to network as taught by Riemann in order to use the network more efficiently.

In regarding to claim 17, Linsley teaches the steps of generating a memory address (Column 4 Line 55-57).

In regarding to claim 18, Munter teaches the steps of receiving cells at an ATM switch 16.

In regarding to claim 19, Munter teaches a scheduler 66, 70 coupled to the memory 58 and a Utopia bus 64.

In regarding to claim 20, Munter teaches a controller 60 determining the location of data storage in the memory 58 (Column 5 Line 37-38).

In regarding to claim 22, Munter teaches the steps of storing data in the serial-to-parallel converters 52 into memory 58 via multiplexer 54 under control of select controller 60 (Column 5 Line 14-19).

In regarding to claim 23, Linsley teaches the steps of incrementing the memory address (Column 4 Line 57-58).

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Munter in view of Linsley and Riemann et al. as applied to claim 20 above and further in view of Shimada. Munter in view of Linsley and Riemann disclosed the steps of converting serial data to parallel data, storing the accumulated words in the memory and reading out the accumulated cells from the memory. Munter in view of Linsley and Riemann, however, does not teach the steps of sending a write enable signal to the memory. Shimada teaches the steps of sending a write enable signal to the memory [0056]. It would have been obvious to one skilled in the art to include the steps of sending a write enable signal as taught by Shimada to Munter in view of Linsley and Riemann in order to initiate the data transfer to the memory.

7. Claim 24-28, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munter in view of Linsley and further in view of Riemann et al..

In regarding to claim 24, Munter teaches the communicating data from a first channel 50 to a first serial-to-parallel converter 52 and communicating data from a second channel 50 to a second serial-to-parallel converter 52. Munter also teaches the converting the first and second sets of data to a parallel format (Column 5 Line 13-14). Munter also teaches the writing data to memory banks 58. Munter also teaches the scheduler 66, 70 reading cells out of the memory banks 58 to an output communication link 64. Munter, however, does not teach the steps of monitoring the serial-to-parallel converters to determine when one or more words of data sets have accumulated. Linsley teaches the steps of waiting for word accumulation in serial-to-parallel converter 21 before writing data into the memory 25 (Column 7 Line 24-26). It would have been obvious to one skilled in the art to modify Munter to have the steps of waiting for the word accumulation before writing data into the memory as taught by Linsley in order to use the memory more efficiently. Munter also does not teach the steps of monitoring the memory to determine when enough of the words have formed cells. Riemann teaches the steps of waiting for cell accumulation in the memory (Column 8 Line 64 – Column 9 Line 2). It would have been obvious to one skilled in the art to modify Munter to

have the steps of waiting for the cell accumulation before reading the data out to network as taught by Riemann in order to use the network more efficiently.

In regarding to claim 25, Linsley teaches the steps of generating a memory address (Column 4 Line 55-57).

In regarding to claim 26, Munter teaches the steps of receiving cells at an ATM switch 16.

In regarding to claim 27, Munter teaches a scheduler 66, 70 coupled to the memory 58 and a Utopia bus 64.

In regarding to claim 28, Munter teaches a controller 60 determining the location of data storage in the memory 58 (Column 5 Line 37-38).

In regarding to claim 30, Munter teaches the steps of storing data in the serial-to-parallel converters 52 into memory 58 via multiplexer 54 under control of select controller 60 (Column 5 Line 14-19).

In regarding to claim 31, Linsley teaches the steps of incrementing the memory address (Column 4 Line 57-58).

8. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Munter in view of Linsley and Riemann et al. as applied to claim 24 above and further in view of Shimada. Munter in view of Linsley and Riemann disclosed the

steps of converting serial data to parallel data, storing the accumulated words in the memory and reading out the accumulated cells from the memory. Munter in view of Linsley and Riemann, however, does not teach the steps of sending a write enable signal to the memory. Shimada teaches the steps of sending a write enable signal to the memory [0056]. It would have been obvious to one skilled in the art to include the steps of sending a write enable signal as taught by Shimada to Munter in view of Linsley and Riemann in order to initiate the data transfer to the memory.

9. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Munter in view of Hoogenboom. Munter teaches the multiplexer 54 receiving data from a first and second channel. Munter also teaches first and second memory banks 58 coupled to the multiplexer. Munter also teaches the scheduler 66, 70 coupled to the memory banks and operable to read out cells out of the memory banks. Munter teaches a controller 60 determining the location of data storage in the memory 58 (Column 5 Line 37-38). Munter, however, does not teach the write controllers to receive parallel data from serial-to-parallel converters. Hoogenboom teaches the write controller 360 coupled to multiple serial-to-parallel converters 333-336 to receive data in parallel form (Column 3 Line 29-30). It would have

been obvious to one skilled in the art to include the write controller as taught by Hoogenboom to Munter in order to increase the control over memory management.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to the ATM communication.

U.S. Patent 5,664,116 to Gaytan et al.

U.S. Patent 6,295,299 to Haddock et al.

U.S. Patent 6,529,523 to Kato

U.S. Patent 6,430,191 to Klausmeier et al.

U.S. Patent 5,323,399 to Kurano


U.S. Patent 5,390,184 to Morris

U.S. Patent 6,215,788 to Sakurai et al.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clemence Han whose telephone number is (703) 305-0372. The examiner can normally be reached on Monday-Friday 8 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703) 308-6602. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-0377.


Clemence Han
Examiner
Art Unit 2665


HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600